

of electrically conductive members; and
forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

95. The method of making the multi-layered interconnect structure of claim 94 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

96. The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;
removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and
forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

97. The method of making the multi-layered interconnect structure of claim 96 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.

REMARKS

Currently pending claims 80-97 are for consideration by the Examiner. Claims 82 and 88 are amended herein.

The Examiner objected to the drawings, alleging "the reference number '26' is pointed to a different part in Fig. 1." In response, Applicants have amended FIG. 1.

The Examiner objected to the disclosure because "on page 16, line 9 the word "pads103" should be --pads 103--. In response, Applicants have amended the disclosure accordingly.

The Examiner objected to the title as allegedly "not being descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested 'METHOD OF MAKING THE ELECTRONIC PACKAGE.'" In response, Applicants have amended the title to be clearly indicative of the invention to which the claims are directed.

The Examiner objected to the Abstract, alleging "the claimed inventions are method claims. Correction is required." In response, Applicants have amended the Abstract accordingly.

The Examiner rejected claims 82 and 88-89 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner rejected claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) as being anticipated by US Patent 4,882,454 to Peterson et al.

The Examiner rejected claims 81, 88, and 92 under 35 U.S.C. §103(a) as being unpatentable over Peterson et al.

The Examiner rejected claims 89 and 90 under 35 U.S.C. §103(a) as being unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeney et al.

Applicants respectfully traverse the §112 and §103(a) rejections with the following arguments.

35 U.S.C. §112, Second Paragraph

The Examiner alleges that “[t]he phrase ‘Laminating .., dielectric layers’ (claim 82, line 4) is vague; examiner does not know how one copper foil being laminated onto two separated dielectric layers.” In response, Applicants have amended claim 82 to clarify the invention.

The Examiner alleges that “[t]he phrase ‘said third dielectric layer’ (claim 88, line 4) lacks of antecedent basis. Examiner notices that this layer has not been formed. In response, Applicants have amended claim 88 to clarify the invention.

35 U.S.C. §102(b)

The Examiner rejected claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) as being anticipated by US Patent 4,882,454 to Peterson et al.

The Examiner alleges: “Regarding claim 80, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102); positioning first (310) and second (311) dielectric layers on the thermally conductive layer; and position first (312) and second (313) pluralities of electrically conductive members on the first and second dielectric layers, each of said first and second pluralities of electrically conductive members adapted for having solder connection (103 and 104) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).”

Applicants respectfully contend that Peterson does not anticipate claim 80, because Peterson does not teach each and every feature of claim 80. For example, Peterson does not

teach "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate".

The Examiner allege that Peterson teaches "the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53)".

In response to the preceding argument by the Examiner, Applicants cite Peterson as stating in col. 2, lines 44- 49 that "[i]deal performance in a surface mount application is achieved when CTE, thermal, weight and electrical properties are optimized by proper choice of materials and geometries. Core modifications can also be made to enhance thermal, CTE or weight properties when specific needs must be met. These involve the use of clad materials in the core, or composite cores of graphite, polymer, and copper." **The preceding disclosure in Peterson is non-specific** and therefore does not disclose specific features of claim 80. While Peterson discloses that optimization could be achieved by "proper choice of materials and geometries", Peterson does not state what is to be optimized and what choice of geometries could be utilized to achieve optimization. For example, Peterson does not specifically disclose optimization "**to substantially prevent failure of said solder connections** between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate" (emphasis added) as required by claim 80. As another example, Peterson does not specifically disclose "said thermally conductive layer being comprised of a material having a **selected thickness** and coefficient of thermal expansion to substantially prevent failure ..." (emphasis added) as required by claim 80.

Based on the preceding arguments, Applicants respectfully maintain that Peterson does not anticipate claim 80, and the claim 80 is in condition for allowance. Since claims 81-86 depend from claim 80, Applicants contend that claims 81-86 are likewise in condition for allowance.

Applicants respectfully contend that Peterson et al. does not anticipate claim 87, because Peterson does not teach each and every feature of claim 87. For example, Peterson does not teach “said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip”. Applicants’ arguments for claim 87 are the same as Applicants’ arguments presented *supra* for claim 80. Based on the preceding arguments, Applicants respectfully maintain that does not anticipate claim 87, and the claim 87 is in condition for allowance. Since claims 88-90 depend from claim 87, Applicants contend that claims 88-90 are likewise in condition for allowance.

Applicants respectfully contend that Peterson et al. does not anticipate claim 91, because Peterson does not teach each and every feature of claim 91. For example, Peterson does not teach “said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate”. Applicants’ arguments for claim 91 are the same as Applicants’ arguments presented *supra* for

claim 80. Based on the preceding arguments, Applicants respectfully maintain that does not anticipate claim 91, and the claim 91 is in condition for allowance. Since claims 88-90 depend from claim 91, Applicants contend that claims 88-90 are likewise in condition for allowance.

Applicants respectfully contend that Peterson et al. does not anticipate claim 91, because Peterson et al. does not teach each and every feature of claim 91. For example, Peterson et al. does not teach... Based on the preceding arguments, Applicants respectfully maintain that Peterson et al. does not anticipate claim 91, and the claim 91 is in condition for allowance. Since claims 92-97 depend from claim 91, Applicants contend that claims 92-97 are likewise in condition for allowance.

35 U.S.C. §103(a)

The Examiner rejected claims 81, 88, and 92 under 35 U.S.C. §103(a) as being unpatentable over Peterson et al, and the Examiner rejected claims 89 and 90 under 35 U.S.C. §103(a) as being unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeney et al. Since claim 81 depends from claim 80, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claim 81 is not unpatentable under 35 U.S.C. §103(a). Since claims 88-90 depends from claim 87, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claims 88-90 are not unpatentable under 35 U.S.C. §103(a). Since claim 92 depends from claim 91, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claim 92 is not unpatentable under 35 U.S.C. §103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 80-97 and the entire application meet the acceptance criteria for allowance, and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact Applicants' representative at the telephone number listed below.

Date: 02/19/2003

Jack P. Friedman

Jack P. Friedman
Registration No. 44,688
Schmeiser, Olsen & Watts
3 Lear Jet Lane
Latham, New York 12110
(518) 220-1850

Appendix A. Identification of Amended Material

Please amend the Abstract as follows:

A[n electronic package, and] method of making [the] an electronic package[, is provided].

The [package] method includes forming a semiconductor chip and an multi-layered interconnect structure. The semiconductor chip includes a plurality of contact members on one of its surfaces that are connected to the multi-layered interconnect structure by a plurality of solder connections. The formed multi-layered interconnect structure is adapted for electrically interconnecting the semiconductor chip to a circuitized substrate (eg., circuit board) with another plurality of solder connections and includes a thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of the solder connections between said first plurality of electrically conductive members and the semiconductor chip. The method forms the electronic package to further include[s] a dielectric material having an effective modulus to assure sufficient compliancy of the multi-layered interconnect structure during operation.

In the specification, please amend the paragraph beginning on page 16, line 8 as follows:

The electronic package of the present invention can be assembled to a circuitized substrate 100 having a plurality of contact pads_103 on one of its surfaces. As described, these contact pads can be comprised of copper or aluminum or another suitable metal and can be coated with a layer of solder paste (not shown). The second plurality of solder connections of the multi-layered interconnect structure, previously described as solder balls or columns 20, are placed in contact with the solder paste on the contact pads of the circuitized substrate. The solder

paste and second plurality of solder connections are reflowed and cooled forming an electrical connection between the multi-layered interconnect structure and the circuitized substrate. The sequence of assembly of the semiconductor chip to the multi-layered interconnect structure, followed by assembly of the multi-layered interconnect structure to the circuitized substrate, can easily be modified so that the multi-layered interconnect structure without the semiconductor chip can be assembled to the circuitized substrate followed by assembly of the semiconductor chip to the multi-layered interconnect structure-circuitized substrate assembly.

Please amend claims 82 and 88 as follows:

82. (Amended) The method of making the multi-layered interconnect structure of claim 80 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a first copper foil and a second copper foil respectively onto said first and second dielectric layers; and

etching selected portions of said first and second copper foils to respectively produce first and second pluralities of said electrically conductive members.

88. (Amended) The method of making the electronic package of claim 87 further comprising positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members, wherein said step of providing said first plurality of solder connections on said first plurality of electrically conductive members includes:

forming a plurality of openings in said third dielectric layer, each of said openings including an internal wall and exposing a portion of at least one of said first plurality of electrically conductive members;

plating a conductive layer on said internal wall of said plurality of openings and on said exposed portion of said at least one of said first plurality of electrically conductive members to define a plurality of microvias;

applying a first solder paste onto said conductive layer; and

reflowing said solder paste to form a first plurality of solder connections.